

## CLAIMS

What is claimed is:

1. A method for selectively etching a high dielectric constant layer over a silicon substrate, comprising:
  - 5 placing the silicon substrate into an etch chamber;  
  
providing an etchant gas into the etch chamber, wherein the etchant gas comprises  $\text{BCl}_3$ , an inert diluent, and  $\text{Cl}_2$ , wherein the flow ratio of the inert diluent to  $\text{BCl}_3$  is between 2:1 and 1:2, and wherein the flow ratio of  $\text{BCl}_3$  to  $\text{Cl}_2$  is between 2:1 and 20:1; and
  - 10 generating a plasma from the etchant gas to selectively etch the high dielectric constant layer.
2. The method, as recited in claim 1, further comprising maintaining the wafer temperature below  $150^\circ\text{C}$  during the etching.
- 15 3. The method, as recited in claim 2, further comprising providing a DC bias of less than 5 volts.
4. The method, as recited in claim 3, further comprising maintaining a pressure  
20 within the chamber to less than 40 mTorr during the etch.

5. The method, as recited in claim 4, wherein the generating a plasma comprises providing more than 700 Watts of Transformer Coupled Power into the etch chamber to energize the etchant gas.

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6. The method, as recited in claim 5, wherein the inert diluent is argon.

7. The method, as recited in claim 6, wherein the etchant gas consists essentially of  $\text{BCl}_3$ , argon, and  $\text{Cl}_2$ .

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8. The method, as recited in claim 7, wherein the selectivity for etching the high dielectric constant layer with respect to silicon is greater than 4:1.

9. The method, as recited in claim 8, where the etch rate of the high dielectric constant layer is between 50-150 Å/minute.

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10. The method, as recited in claim 9, wherein the high dielectric constant layer has a dielectric constant of at least 8.

11. The method, as recited in claim 1, further comprising providing a DC bias with an absolute value of less than 5 volts.

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12. The method, as recited in claim 1, further comprising maintaining a pressure within the chamber to less than 40 mTorr during the etch.
13. The method, as recited in claim 1, wherein the inert diluent is argon.
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14. The method, as recited in claim 1, wherein the etchant gas consists essentially of  $\text{BCl}_3$ , argon, and  $\text{Cl}_2$ .
15. The method, as recited in claim 1, wherein the selectivity for etching the high dielectric constant layer with respect to silicon is greater than 4:1.
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16. The method, as recited in claim 1, where the etch rate of the high dielectric constant layer is between 50-150 Å/minute.
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17. The method, as recited in claim 1, wherein the high dielectric constant layer has a dielectric constant at least 8.
18. A method for forming a semiconductor device, comprising:
- forming a high dielectric constant layer over a substrate;
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- forming a poly-silicon layer over the high dielectric constant layer;
- forming a patterned mask over the poly-silicon layer;
- etching a feature into the poly-silicon layer through the patterned mask;

etching the high dielectric constant layer to expose the substrate not under the patterned mask, comprising the steps of:

providing an etchant gas, wherein the etchant gas comprises  $\text{BCl}_3$ , an inert diluent, and  $\text{Cl}_2$ , wherein the flow ratio of the inert diluent to  $\text{BCl}_3$  is between 2:1 and 1:2, and wherein the flow ratio of  $\text{BCl}_3$  to  $\text{Cl}_2$  is between 2:1 and 20:1; and

generating a plasma from the etchant gas to selectively etch the high dielectric constant layer; and

performing an ion implantation into the exposed substrate.

10 19. The method, as recited in claim 18, further comprising maintaining the wafer temperature below  $150^\circ\text{C}$  during the etching.

20. The method, as recited in claim 18, further comprising providing a DC bias with an absolute value of less than 5 volts.

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